CLAIMS:

1. A variable size first in first out (FIFO) memory comprising:

   a head FIFO memory for sequentially delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between data packets:

   a tail FIFO memory for storing an overflow of said data packets from said head memory; both said head and tail memories operating at a relatively high data rate equivalent to the rate of incoming data packets;

   a large capacity buffer memory having an effectively lower clock rate than said FIFO memories for temporarily storing data overflow from said tail memory whereby said FIFO memories in combination with said buffer memory for a variable size FIFO memory.

2. A memory as in claim 1 where said head and tail memories have data blocks of a predetermined and same size and said buffer memory has the same size data block whereby high efficiency data transfer between memories is obtained.

3. A memory as in claim 1 where FIFO memories reside on a common semiconductor substrate and said buffer memory is remote.

4. A memory as in Claim 1 where said buffer memory has a wider bus than said head and tail FIFO memories.